

Real-Time Soft-Error Rate (SER) Testing

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Outline

- Introduction Context Basic mechanisms
- Test platforms Platform characteristics
- Devices under test
- Automatic Test Equipment
- Experimental results
- Comparison with accelerated tests and simulations
- Conclusions & perspectives



Introduction - Context

Pionnering work by Ziegler and co-workers (IBM) in the 70s and 80s



J.F. Ziegler et al. *IBM experiments in soft fails in computer electronics (1978-1994)* IBM J. Res. Develop., Vol. 40, Number 1, 1998





Pb,Sn solder bump Underfill Random emissions Sensitive memory cells

Introduction - Context

Electronic devices at ground level are primilarly impacted by:

 Secondary cosmic rays in the Earth atmosphere (neutrons)

 ✓ Telluric ray produced directly inside ICs due to residual traces (≤ ppB) of radioactive elements (alpha particles)

• Neutrons and alpha particles are the main aggressors playing a major role in the occurrence of SEE in SRAMs at ground level







/_{diff}

Main steps of SEE production in microelectronic devices (2/2)*

I_{drift}



Charge deposition by the energetic particle striking the sensitive region

 $\mathbf{1}$

Transport of the released charge into the device (drift and diffusion mechanisms)

Charge collection in the sensitive region of the device



* After R. C. Baumann, *IEEE Trans. Device Mater. Reliab*., vol. 5(3), p. 305-316, Sept. 2005.



Charge deposition, transport and collection occur in a <u>high complexity media</u> : the CIRCUIT







Introduction – Terminology



* JEDEC Standard JESD89A

Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices, <u>http://www.jedec.org/download/search/JESD89A.pdf</u>



SEU = **Single Event Upset** (SRAM memory)



Snapshots courtesy of P. Roche



DSET = <u>Digital Single Event Transient</u>

= constitute a <u>temporary voltage or current transient</u> generated by the collection of charge deposited by an energetic particle in a digital circuit



Even if the DSET does not induce an SEU in the struck circuit, it can **propagate** through the subsequent circuits and may be stored as incorrect data **when it reaches a latch or memory element**





P. Shivakumar et al., in Proc. Int. Conf. Dep. Systems & Networks, DSN 2002.



Introduction - Context

⇒ <u>Objective of this work</u>: perform real-time testing of SRAMs to evaluate neutron and alpha particle-induced SER Verify once during the technology qualification phase that both accelerated testing and simulation are accurate

<u>Principle of the experiment</u>: long-term (several months) exposure of a large amount (Gbits) of circuits to the natural radiation environment

- In altitude: to amplify the atmospheric neutron flux (typically by a factor of 3 to 15 at ground level)
- Underground: to remove the atmospheric neutron contribution (observed soft-errors are expected to be due to alpha particles)



Test platforms





-1700 m under rock





+2552 m in Alp mountains





ASTEP, Plateau de Bure, France						
Latitude (°N)	44.6					
Longitude (°E)	5.9					
Elevation (m)	2552					
Atm. depth (g/c	757					
Cutoff rigidity (5.0					
Relative	Active Sun low	5.76				
neutron	Quiet Sun peak	6.66				
flux	Average	6.21				

The Altitude SEE Test European Platform







XILINX "Rosetta" Experiment hosted by ASTEP XILINX[®]

> ASTEP System-SER

www.astep.eu

ASTEP main control PC (internet firewall, weather monitoring, control webwam...)





The Modane Underground Laboratory (LSM)





ULTRA LOW NOISE ENVIRONMENT

- Depth: 4800 m water equivalent
- 4×10⁻⁶ neutrons/cm²/s [2-6 MeV]

4.2 muon/m²/day

Radon < 20 mBq/m³

Residual radioactive activity:

	²³⁸ U	²³² TH	⁴⁰ K
Mountain	(0.84±0.2)	(2.45±0.2)	(0.213±0.03)
roc	ppm	ppm	Bq/g
Tunnel	(1.9±0.2)	(1.4±0.2)	(7.73±1.3) 10 ⁻²
concrete	ppm	ppm	Bq/g



Devices under test

- SRAM test vehicle designed and manufactured by STMicroelectronics in CMOS 130 nm
- Fully characterized and simulated testchip :
 - ✓ *alphas* (ST and IM2NP with Am²⁴¹)
 - Instrument of the second se
 - TCAD (ST with Synopsys tool suite)
 - SER Simulation (proprietary codes)
- 4 Mbits per device
- 912 devices
- Total capacity > 3.6 Gbits



Bitcell area = 2.50 μm²



The Automatic Test Equipment (ATE)



- Data writing (32 bits) with selected pattern
- For each memory point, Writing and rereading with data control
- If data correct, go test the next memory point
- If data state not correct, try to reread twice the data
- If data correct after rereading, error identified as "Transient Soft Error"
- If data still not correct, test twice to rewrite and to reread.
- If control valid after rewriting and rereading, error identified as "Static Soft Error"
- If control not valid after rewriting and rereading, error identified as "Single-Event Hard Error"

Frror list of Rack 1 : Mother board 1 : Daughter board 1 : Memory 1

Date	Heure	Temp.	Туре	Write	Read	G.address	M.address
11/03/05	10:30:00	85° C	TSE	55555555	55555554	10000000	00000
11/03/05	10:30:01	85° C	TSE	AAAAAAAA	٨٨٨8٨٨٨	10040005	00005
11/03/05	10:30:01	84° C	TSE	FFFFFFF	FFFFEFFF	10A60100	00100
11/03/05	10:30:02	84° C	TSE	00000000	10000000	13F84539	04539
11/03/05	10:30:03	84° C	SSE	7777777	7x777277	14720123	00123
11/03/05	10:30:04	85° C	SSE	55555555	555x5555	14720124	00124
11/03/05	10:30:04	86° C	TSE	<u>مممممممم</u>	ΑΑΑΑΒΑΑΑ	14761234	01234
11/03/05	10:30:04	90° C	SEHE	FFFFFFF	xFFFFFF1	15256789	16789
11/03/05	10:30:05	95° C	SEHE	00000000	00F00x00	15256790	16790
11/03/05	10:30:05	98° C	VDD 2			16080000	

Exit







Daughtercard (×640)

Chip(×1280)



Experimental Results

Number of fails measured in both altitude and cave during 216 days (>7 months)





Experimental Results

Soft-Error Rate measured in both altitude and cave

Neutron-SER cannot be directly extracted due to alpha contribution Data directly gives access to alpha-SER (neutron contribution negligible)

Experimental Results

Neutron and alpha-SER extraction

Comparison with accelerated tests

• Alpha SER

- Real-time @ LSM (this work)
- Accelerated test @ ST (1)

1530 FIT/Mbit

380 FIT/Mbit

(1) Using an Am²⁴¹ α-source and assuming an alpha-emissivity of <u>10⁻³ α/cm²/h</u> for the semiconductor processing and packaging materials
 α-counting measurements using gas proportional counters @ ST give ~2×10⁻³ α/cm²/h

 \Rightarrow Real-time testing @ LSM allows us to more accurately quantify the α -emission rate for the chip materials:

 $10^{-3} \times (1530/380) = \frac{4 \times 10^{-3} \alpha / cm^2 / h}{10^{-3} \alpha / cm^2 / h}$

⇒ Confirms the ultra-low alpha-emission level of chip materials within the experimental error margins for the α-counting and lot-to-lot variations

Comparison with accelerated tests and SER simulation

- Neutron SER
 - ✓ Real-time @ ASTEP (this work)
 - ✓ Accelerated test @ TRIUMF [1]
 - ✓ 3D SER simulation [2]

504 FIT/Mbit 665 FIT/Mbit 700 FIT/Mbit

⇒ Values in good agreement (±15%) within the experimental error margins for the different techniques

[1] J.L. Autran et al. IEEE Transactions on Nuclear Science, 2007, Vol. 54, n°4, p. 1002-1009.
[2] P. Roche et al., IEEE Transactions on Nuclear Science, 2003, Vol. 50, N°6, pp. 2046-2054.

Conclusion

- This work: real-time soft-error rate testing of 3.6 GBits of bulk 130 nm SRAMs in both altitude and underground environments.
- Combination of these two tests allowed us to separate the components of the SER induced by atmospheric neutrons from that caused by on-chip alpha-particle emitters.
- Here, the alpha contribution is found to be three times larger than the neutron contribution at sea-level.
- This work shows the importance of combining real-time, accelerated and α-emission characterizations, to accurately quantify the soft-error rate of a given technology.
- Such a multi-characterization approach should ensure that the different extracted values are consistent with the underlying calculation hypothesis and are within experimental error margins.

Perspectives

Simultaneous measurements of SER and cosmic-ray neutron flux

→ IM2NP recently developed a high performance neutron monitor (super 3-NM64) to provide in situ and real-time data of the atmospheric neutron flux impacting SER experiments on the ASTEP Platform.

Perspectives

New combined Altitude/Cave experiment (currently in progress) on 65nm Bulk SRAMs with 2 identical setups

The 65nm setup at ASTEP Experiment started on January 21, 2008

The 65nm setup at LSM Experiment started on April 11, 2008

Acknowledgments

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